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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/801,564	SAULSBURY ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2005 and 10 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-13 and 15-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-13 and 16-24* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 06/14/2005 and 01/10/2005.

2. Claims 1-2, 4-13, and 15-24 are pending in this application. Claims 1, 9, and 18 are independent claims. This Office Action is made non-final after a RCE filed 05/05/2005.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 4-5, 7, and 18-20 are rejected under 35 U.S.C. 103(a) as being obvious over Lin et al. (U.S. 5,959,874) in view of Nakakimura et al. (U.S. 5,915,109).

Re claim 1, Lin et al. disclose in Figures 1, 4a, 6-7, 9, 12, and 16-17 a processing core (e.g. 100 in Figure 1) comprising: a first source register (e.g. Figure 6 and Figure 7a) including a plurality of first operands (e.g. 705a and 705b wherein each SRC1 is subdividing into plurality of operands such as $Source1_{7-0}$; $Source1_{15-8}$...); a plurality of second operands (e.g. 705a and 705b wherein each SRC2 is subdividing into plurality of operands such as $Source2_{7-0}$; $Source2_{15-8}$...), wherein: the plurality of second operands are equal in value to an immediate value (e.g. throughout the specification of the cited patent, all the elements/operands in SRC2 can be set to be equal in a value), a bitwise

inverter coupled to at least one of the first plurality of operands and the second plurality of operands (e.g. 1603 in Figure 16 for performing subtraction operation); a destination register including a plurality of results (e.g. col. 2 lines 50-63 and 910a-910c in Figure 9); a plurality of arithmetic processors (e.g. 907a-907h in Figure 9) respectively coupled to the first operands, second operands and results (e.g. Source1, Source2, and ResultOut respectively in each of 907a-907h in Figure9), wherein each arithmetic processor computes one of a sum (e.g. adder label 908a in Figure 9).and a difference (e.g. subtractor label 908a in Figure 9) of the first operand and a respective second operand (e.g. either addition or subtraction in Figure 9). Lin et al. fail to disclose the immediate value is specified in an instruction that identifies the first source register. However, Nakakimura et al. disclose in Figure 3 a kind of instruction that identifies the first source register (e.g. Ra/Rb in Figure 3) and also the immediate value (e.g. 118 in Figure 3). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the immediate value specified in the same instruction that identifies the first operand as seen in Nakakimura's Figure 3 into Lin et al.'s invention because it would enable to direct access immediate value without addressing which would leads to improve the overall system performance (e.g. col. 7 lines 20-25 and col. 8 lines 20-26).

Re claim 2, Lin et al. further disclose in Figures 1, 4a, 6-7, 9, 12, and 16-17 an integrated circuit (e.g. 100 in Figure 1) which includes the first source register (e.g. SRC1 in 702 of Figure 7a), destination register (e.g. DEST in 706 of Figure 7a) and arithmetic processor (e.g. 109 in Figure 1 and particular function as seen in Figures 7a and 9).

Re claim 4, Lin et al. further disclose in Figures 1, 4a, 6-9, 12, and 16-17 each arithmetic processor (e.g. 907a-907h in Figure 9) computes at least one of: the result of the first operand plus another operand plus the immediate value (e.g. 1706 in Figure 17 wherein the first operand is the first packed data; the another operand is the carry-in; and the immediate value is the third packed data); and the result of the first operand minus another operand minus the immediate value (e.g. similarly for subtractor in Figure 9); and each of the first operand, the another operand and the immediate value are represented with a plurality of bits (e.g. each of first and immediate value are plurality of bits as seen in Figure 7a; the another operand is carry-in bits for each of single bit add/subtractor as seen in Figure 8, the arithmetic processor in Figure 9 is 8-bits, thus it needs 8 carry-in bits).

Re claim 5, Lin et al. further disclose in Figures 1, 4a, 6-7, 9, 12, and 16-17 the immediate value is signed (e.g. format in Figure 5b and wherein it requires either one/two complement for operation as seen in Figure 17 step 1703, this claim is incorporated into claim 1 for consideration).

Re claim 7, Lin et al. further disclose in Figures 1, 4a, 6-7, 9, 12, and 16-17 a first width of the first source register is a positive integer multiple of a second width of the first operand (e.g. abstract lines 5-6 and Figure 5b).

Re claim 18, it is a method claim of claim 1. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claims 19-20, Lin et al. in view of Nakakimura et al. do not disclose the immediate value comprises either nine or thirteen bits. However, it is obvious to

application choice to have the immediate value has a width of nine or thirteen bits. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the width of the immediate value of nine or thirteen bits into Lin et al. in view of Nakakimura et al.'s invention because it would enable to reduce the system circuitry for that particular application needs.

5. Claims 6, 9-10, 12-13, 16, and 21-22 are rejected under 35 U.S.C. 103(a) as being obvious over Lin et al. (U.S. 5,959,874) in view of Nakakimura et al. (U.S. 5,915,109), as applied to claim 1 above, and further in view of Pineda (U.S. 5,701,263).

Re claim 6, Lin et al. in view of Nakakimura et al. do not disclose a processing core comprising a prescaler, which scales the immediate value. However, Pineda discloses in Figures 2 and 7 a processing core comprising a prescaler, which scales input values (e.g. 204 in Figure 2 and 702 in Figure 7). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a prescaler for scaling the input value as seen in Pineda's Figures 2 and 7 into Lin et al. in view of Nakakimura et al.'s invention because it would enable to simplify the arithmetic operation (e.g. col. 2 lines 5-11 and lines 15-30, and col. 3 lines 40-45).

Re claim 9, it is a method claim of claim 6. Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 10, Lin et al. further disclose in Figures 1, 4a, 6-7, 9, 12, and 16-17 a step of inverting the third and fourth operands (e.g. 1603 in Figure 16).

Re claim 11, Lin et al. further disclose in Figures 1, 4a, 6-7, 9, 12, and 16-17 a step of adjusting at least one of the first and second results to avoid saturation of the destination register (e.g. 703 in Figure 7a as saturation applied).

Re claim 12, it has method limitations as cited in claim 4. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 13, it has method limitations as cited in claim 4. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 16, Lin et al. further disclose in Figures 1, 4a, 6-9, 12, and 16-17 the two performing steps are performed (e.g. 801a and 801b in Figure 8), at least partially, coextensive in time (e.g. Figures 8-9).

Re claim 21, it has same method limitations as cited in claim 16. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 16.

Re claim 22, it has same method limitations as cited in claim 11. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being obvious over Lin et al. (U.S. 5,959,874) in view of Nakakimura et al. (U.S. 5,915,109), as applied to claim 1 above, and further in view of Beck et al. (U.S. 3,993,891).

Re claim 8, Lin et al. further disclose in Figure 9 the sum and the difference are performed on a same adder (e.g. 907a-907h in Figure 9). Lin et al. in view of Nakakimura et al. fail to disclose the adder is carry look-ahead adder. However, Beck et al. disclose in Figure 6 a carry look-ahead adder is used to perform add/subtract (e.g. col.

8 lines 55-65). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the carry look-ahead adder as seen in Beck et al.'s Figure 6 into Lin et al. in view of Nakakimura et al.'s invention because it would enable to increase the large system performance (e.g. abstract).

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being obvious over Lin et al. (U.S. 5,959,874) in view of Nakakimura et al. (U.S. 5,915,109) and Pineda (U.S. 5,701,263), as applied to claim 9 above, and further in view of Beck et al. (U.S. 3,993,891).

Re claim 17, Lin et al. in view of Nakakimura et al. and Pineda fail to disclose the adder is ripple look-ahead adder. However, Beck et al. disclose in Figure 6 a ripple look-ahead adder is used to perform add/subtract (e.g. col. 8 lines 55-65). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the ripple look-ahead adder as seen in Beck et al.'s Figure 6 into Lin et al. in view of Nakakimura et al. and Pineda's invention because it would enable to increase the large system performance (e.g. abstract).

8. Claim 23 is rejected under 35 U.S.C. 103(a) as being obvious over Lin et al. (U.S. 5,959,874) in view of Nakakimura et al. (U.S. 5,915,109), as applied to claim 1 above, and further in view of Phillips Inc. ("An Introduction to Very-Long Instruction Word (VLIW) Computer Architecture").

Re claim 23, Lin et al. in view of Nakakimura et al. do not disclose the instruction is VLIW instruction. However, Phillips Inc. discloses the VLIW instruction (e.g. pages

2-6). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the VLIW instruction as seen in Phillips Inc.'s article into Lin et al. in view of Nakakimura et al.'s invention because it would enable to process multiple operations concurrently and simpler and cheaper to implement (e.g. page 3 last paragraph of "why VLIW" section).

9. Claim 24 is rejected under 35 U.S.C. 103(a) as being obvious over Lin et al. (U.S. 5,959,874) in view of Nakakimura et al. (U.S. 5,915,109) and Pineda (U.S. 5,701,263), as applied to claim 9 above, and further in view of Phillips Inc. ("An Introduction to Very-Long Instruction Word (VLIW) Computer Architecture").

Re claim 24, Lin et al. in view of Nakakimura et al. and Pineda do not disclose the steps are initiated by a single instruction issue. However, Phillips Inc. discloses the single VLIW instruction (e.g. pages 2-6) for performing or initiating multiple steps. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the single VLIW instruction for performing multiple steps as seen in Phillips Inc.'s article into Lin et al. in view of Nakakimura et al. and Pineda's invention because it would enable to process multiple operations concurrently and simpler and cheaper to implement (e.g. page 3 last paragraph of "why VLIW" section).

Allowable Subject Matter

10. Claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

11. Applicant's arguments with respect to claims 1-2, 4-13, and 16-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,016,543 to Suzuki et al. disclose a microprocessor for controlling the conditional execution of instructions.

b. U.S. Patent No. 6,397,235 to Van Eijndhoven et al. disclose a data processing device and method of computing the costine transform of a matrix.

c. U.S. Patent No. 6,408,320 to Shiell discloses an instruction set architecture with versatile adder carry control.

d. U.S. Patent No. 6,839,728 to Pitsianis et al. disclose an efficient complex multiplication and fast Fourier transform (FFT) implementation on the manarray architecture.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

August 8, 2005